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REMARKS

Claims 1, 3-8, 10-15, and 17-20 are all the claims pending in the application. The limitations of dependent claims 2, 9, and 16 have been incorporated into their associated dependent claims 1, 8, and 15 and dependent claims 2, 9, and 16 have been correspondingly cancelled. The foregoing does not raise a new issue requiring further consideration or search but instead merely incorporates previously considered and previously searched features from dependent claims into independent claims. Therefore, entry of this Amendment is proper. Claims 1, 3-8, 10-15, and 17-20 stand rejected on prior art grounds. Applicants respectfully traverse these objections/rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hsu et al., hereinafter "Hsu" (US Patent Publication 2002/0171101 A1) in view of Holst (U.S. Patent No. 6,054,918). Applicants respectfully traverse these rejections based on the following discussion.

A. The Rejection Based on Hsu in view of Holst

Applicants respectfully traverse this rejection because neither applied reference (alone or combined) teaches that the connection of only one of the complementary transistor's source regions to ground programs the ROM cell. Hsu does not disclose altering physical connections in order to program the devices and Holst discloses changing the connection to the bitline (not the ground connection) to program the device. Therefore, neither reference discloses programming through the selective connection of only one of the transistors to ground as in the claimed invention.

Hsu discloses a memory cell structure, in Figure 2 for example, that includes separate transistors C1, C2 connected to true and complement bitlines. The Office Action

admits that Hsu does not teach altering the source connection to ground. Therefore, the Office Action makes reference to Holst for teaching such a feature.

However, Holst is fundamentally different than the claimed invention because Holst changes the connection between the drains and the bitlines to program the transistors. For example, as shown in Figure 8 of Holst, the first two sets of transistors 804-806 and 814-816 are programmed and contain connections to the bitlines. To the contrary, transistors 824, 826 are not connected to the bitlines and are therefore unprogrammed. Therefore, Holst programs its transistors by selectively forming connections between the drains and the bitlines. Applicants' Figure 1 shows that Applicants' invention programs the transistor pair by connecting only one of the transistors to ground.

More specifically, as shown in Applicants' Figure 1, a logical 0 is achieved by having the source of the true transistor connected to ground, while the source of the complementary transistor is left floating. To the contrary, a logical 1 is achieved by having the source of the true transistor electrically insulated (floating), while the source of the complementary transistor is tied to ground. Therefore, the cell 100 represents a logical 0 because the source 117 of the complementary transistor 115 is left floating, while the source 110 of the true transistor 111 is tied to ground 104. To the contrary, cell 101 represents a logical 1 by having the source 123 of the true transistor 120 floating and the source 122 of the complementary transistor 121 connected to ground 107.

In operation, both true and complement bitlines are precharged to VDD. When the wordline voltage rises, the transistors connected to ground will conduct and pull its respective bitline towards ground. The transistor that has its source floating will have no affect on its respective bitline which should maintain a voltage near VDD. If the true transistor pulls the true bitline towards ground while the complement bitline remains near VDD, a logical 0 is read. If the complement transistor pulls the complement bitline towards ground while the true bitline remains near VDD, a logical 1 is read. Note also that, since drains are always connected to the bitlines, all bitlines will have approximately the same capacitance.

These features are clearly defined by independent claims 1, 3, 8, 10, 15 and 17 which state "a connection of one of said first source and said second source to a ground programs said ROM cell" using substantially similar language.

In view the forgoing, Applicants respectfully submit that independent claims 1, 3, 8, 10, 15 and 17 are patentable over Hsu and Holst because neither teaches or suggests that "a connection of one of said first source and said second source to a ground programs said ROM cell." Further, not only are independent claims 1, 3, 8, 10, 15 and 17 patentable, but also, dependent claims 2, 4-7, 9, 11-14, 16, and 18-20 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also of because of the additional features of the invention they define. In view the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

II. Formal Matters and Conclusion

With respect to the objection to the drawings, Applicants previously filed formal drawings on May 2, 2002. A courtesy copy of those drawings is attached hereto. In view the foregoing, the Examiner is respectfully requested to reconsider and withdraw the objection to the drawings.

In view of the foregoing, Applicants submit that claims 1, 3-8, 10-15, and 17-20, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

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Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: 9/30/03

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